thin film technology for microelectronics

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Thin film products for microelectronics

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Technical Specification

Version No.: 12 Date: 01.04.2007

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Substrates

for thin film technology

Product Specification —— *Data Sheet No. RMT-SH-A-679-01-010407*

STANDARD SUBSTRATE TYPES

Substrate Type & Code	Al_2O_3 99,6%			Al_2O_3 96%		ALN
	CoorsTek ADS 996	CoorsTek Superstrate 996	Kyocera A493	CoorsTek ADS 96R	Ceramtec R708S	Aluminum Nitride

Dimensions and Tolerances, [1)]

Dimensions (L x W)	**2"x2" to 4"x 4" and 3,75"x4,5" (Herman Size)**					
Standard	± 1.0%					
Select	± 0.5%					
As fired	**A996**	**MRCA**	**A493**	**A96**	**R708**	**ALN**
Thicknesses	**0.005" / 0.010" / 0.015" / 0.025" / 0.050"**					
Standard	± 10%			± 10%		
Select	± 5%			± 7%		
Camber	**0.002 to 0.003 "/" (inch per inch)**					
Standard	0.002"/"		0.003"/"	0.003"/"		
Select	0.002"/"			0.002"/"		
Surface properties [1)]						
Roughness Ra, A-side only [2)]	≤ 3µ"	≤ 2µ"	≤ 3µ"	≤ 35µ"	≤ 25µ"	≤ 25µ"
Burrs diameter ≤	0.005"			0.010"		
Pits diameter ≤	0.005"			0.010"		
Scratches depth ≤	0.0002"			0.0007"		
Chips width ≤	0.75% of substrate length			1% of substrate length		
Bumps, Cracks, Riges	none			No cracks, ridges < 0.001"		none
Lapped	**A996L**	**MRCL**	**A493L**	**A96L**	**R708L**	**ALNL**
Thicknesses	**0.005" to 0.050"**					
Standard	± 0.002"					
Select	± 0.001"					
Surface properties [1)]						
Roughness Ra [2)]	12µ" to 20µ"					
Microvoids none	> 25µm			n/a		> 25µm
Polished	**A996P**	**MRCP**	**A493P**	**A96P**	**R708P**	**ALNP**
Thicknesses	**0.005" to 0.050"**					
Standard	± 0.0010"			n/a		± 0.0010"
Select	± 0.0005"					± 0.0005"
Flatness & Parallelism						
Standard	0.0010"/"			n/a		0.0010"/"
Select	0.0005"/"					0.0005"/"
Surface properties [1)]						
Roughness Ra [2)]	< 1µ"			n/a		< 2µ"
Microvoids none	> 20µm					> 20µm
(d=diameter in µm) 20/in²	> 10µm					> 10µm
150/in²	> 5µm					> 5µm

Physical properties

Characteristic	Units	A996..	MRCA..	A493..	A96..	R708..	ALN..
Al_2O_3/ALN content	Wt.%	99.6%			96%		>95
Density	g/cm³	3.88	3.88	3.85	3.75	3.78	3.30
Grain size	µm	<1.2	<1.0	<1.5	4-7	3-5	~ 5
Flextural strength	N/mm²	592	620	550	400	500	300
Thermal expansion	K^{-1}	~ $7x10^{-6}$			$6.4x10^{-6}$	$6.8x10^{-6}$	$4.6x10^{-6}$
Thermal conductiv.	W/mK	~ 35 (@ 25°C)			~ 25 (@ 100°C)		170 (@ 25°C)
Dielectric strength	kV/mm	~ 23			~ 20		~ 15
Volume resistivity	Ω.cm	> 10^{-14}					> 10^{-12}
Dielectric constant	@ 1MHz	9.9			9.5		8.5-9.2
-"-	@10GHz	9.5	9.6	9.5	n/a		n/a
Loss tangent	@ 1MHz	0.0001			0.0004		0.0004
-"-	@10GHz	0.0002			n/a		n/a

1) On full substrates guaranteed up to 5mm from the substrate edge — 1µ" = 0.025_4 µm

2) CLA according to ANSI/ASME B46.1 (DIN 4768), guaranteed on front side (as fired) or both sides (lapped, polished), uncertainty ±0,5µ",k=2

Features not covered herein might be available on request.

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Substrate 1737G

Corning / 1726G / as drawn

Alkaline Earth Aluminoborosicate Glass

Product Specification — *Data Sheet No. RMT-SH-A-528-01-010702*

STANDARD DIMENSIONS

(others on request)

Sizes:

2" x 2"	(50.8 mm x 50.8 mm)
3" x 3"	(76.2 mm x 76.2 mm)
4" x 4"	(101.6 mm x 101.6 mm)

Thicknesses:

0.020"	(0.5 mm)
0.043"	(1.1 mm)

QUALITY LEVEL

Tolerances on dimensions:

Length		± 0.015"	(0.38 mm)
Width		± 0.015"	(0.38 mm)
Edges		score cut	
Squareness		90° ± 1°	
Thickness	0.020"	± 0.002"	(0.05 mm)
	0.043"	± 0.004"	(0.10 mm)
Warp		≤ 0.1%	of the longer substrate edge
Flatness		< 3.5 µm	over 25 mm
Surface finish (Ra)		0.25	µinch

Visual defects:

Digs and pits	> 0.005"	none
Inclusions	> 0.005"	none
Scratches (at 1.5 KLux illumination)	visible with naked eye	none
Edge chips	≤ 0.060"	long
	≤ 0.015"	wide

COMPOSITION

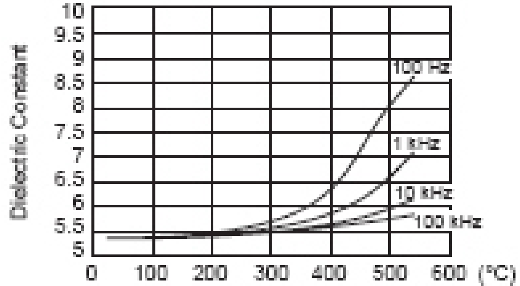
(percent by weight, present as oxides)

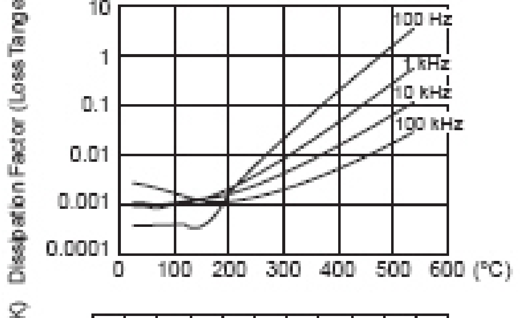
Si	< 30 %	B	< 5 %	Ca	< 5 %
Ba	< 10 %	Sb	< 5 %	Mg	< 1 %
Al	< 10 %	Sr	< 5 %	Alcali	< 0.1 %

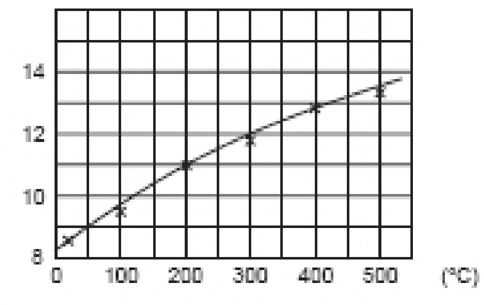
PHYSICAL PROPERTIES

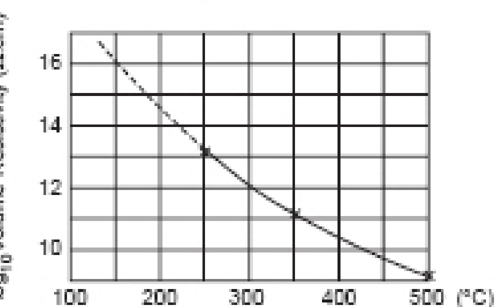
(specified by Manufacturer)

Density	2.54	g/cm³
Thermal expansion (0 - 300°C)	3.85×10^{-6}	$°C^{-1}$
Softening point	978	°C
Annealing point	721	°C
Strain point	666	°C
Young's modulus	7.2×10^4	N/mm
Shear modulus	2.86×10^4	N/mm
Poisson's ratio	0.26	
Refractive index (Sodium D-line)	1.53	









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Substrate SW

Silicon Wafer / polished / oxidized

Product Specification — *Data Sheet No. RMT-SH-A-342-02-010702*

DIMENSIONS

	3"		100 mm	
	Test	Prime	Test	Prime
Diameter	3 ± 0.05"	3 ± 0.025"	100 ± 2 mm	100 ± 0.5 mm
Thickness	0.015 ± 0.002"	0.015 ± 0.001"	525 + 50 µm / - 90 µm	525 ± 25 µm
Bow	not specified	< 40 µm	not specified	< 40 µm

According to SEMI Standard

QUALITY LEVEL

	3"		100 mm	
	Test	Prime	Test	Prime
Front side	polished	polished	polished	polished
Scratches Max number per wafer Max total length per wafer	 5 1.5"	 3 0.75"	 5 50 mm	 3 25 mm
Contamination/particulate Max number per wafer	 9	 6	 16	 10
Edge chips (> 0.010") Max number per wafer	 4	 none	 4	 none
Cracks, fractures	none	none	none	none

According to SEMI Standard and ASTM method F523 and F154.

OTHER INFORMATION

Growth method	Float zone
Back surface	Etched
Additional treatment	Both sides oxidized with 1.5 µm ± 10% thermal SiO_2

PHYSICAL PROPERTIES OF Si

Density	2.33	g/cm^3	
Knoop hardness	850	kg/mm^2	
Thermal expansion	$2.33\ 10^{-6}$	K^{-1}	at 25 °C
Dopant	not specified		
Orientation	not specified		
Thermal conductivity	113	W/mK	at 25 °C
Volume resistivity	> 1000	Ω cm	

PHYSICAL PROPERTIES OF SiO_2

Dielectric strength	1	kV
Volume resistivity	10^{+16}	Ω cm
Index of refraction	1.46	

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Thin Film Resistive Layers

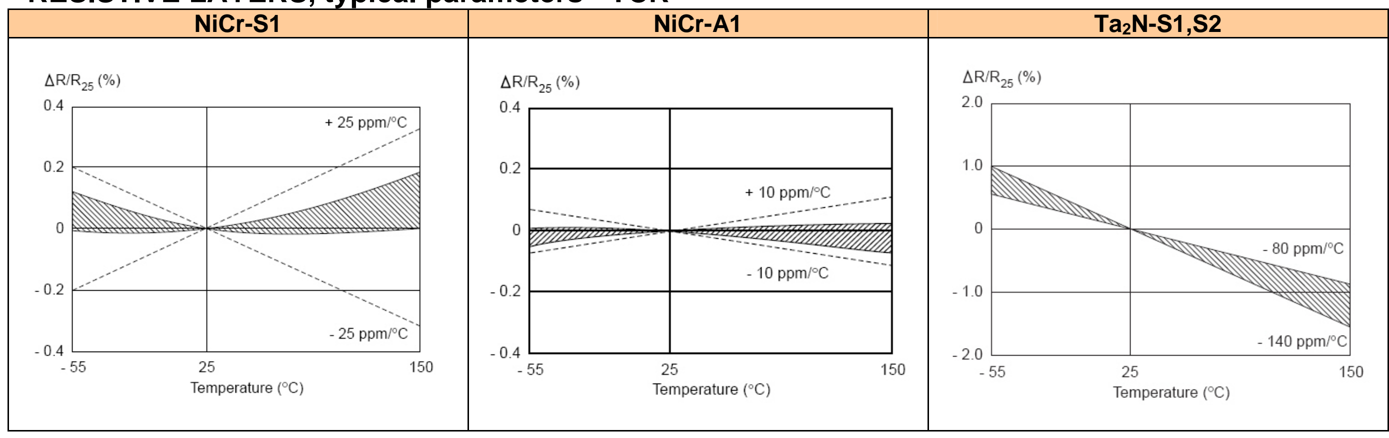
on substrate or adhesive layer

Product Specification — *Data Sheet No. RMT-SH-A-680-01-010407*

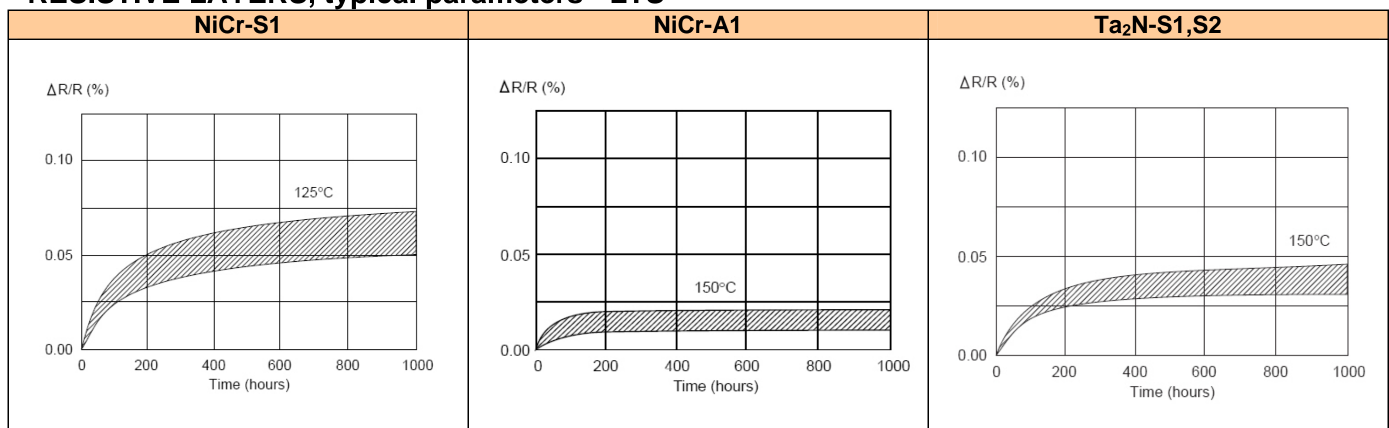
RESISTIVE LAYERS, sputtered 1)

Standard	Sheet resistance range		Sheet resistance deviation			TCR 2)		LTS 3)		
	Substrate type	Range (Ω / □)	Stabilisation bake	Nominal %	Batch %	Absolute ppm/°C	Tracking ppm/°C	storage @ °C	change max. %	Tracking max. %
NiCr-L	Alumina as fired/polished	20 - 200	n/a							
NiCr	ALN polished Glass, Si-Wafer	20 - 200	300°C/2h	±15	±10	± 50	≤ 10	125	0.20	0.03
NiCr-S1	Alumina as fired/polished	20 - 250		±14	±6	± 25	≤ 5		0.10	0.01
	Glass, Si-Wafer	20 - 300		±10	±4					
NiCr-S2	Alumina as fired/polished	20 - 150		±10	±5	± 15	≤ 3			
	Glass, Si-Wafer	20 - 250		±6	±3					
NiCr-A0	Alumina as fired/polished	50 - 250		±10	±5	± 25	≤ 5		0.08	0.01
NiCr-A1			350°C/2h	±10	±5	± 10	≤ 2	150	0.03	0.006
Ta_2N-S1		20 - 150		±14	±6	-80 to -140	≤ 5		0.05	0.02
Ta_2N-S2				±10	±5					
Ta_2N	Alumina as fired/polished ALN polished	20-150	300°C/2h	±15	±10	n/a				

RESISTIVE LAYERS, typical parameters - TCR



RESISTIVE LAYERS, typical parameters - LTS



1) **Values** are guaranteed 2σ after recommended annealing up to 5mm from the edge of the metallised substrate
2) **TCR** - Temperature Coefficient of Resistance as function of temperature, acc. to MIL-Std 202, Method 304, within –55 to +150°C
3) **LTS** - Long Term Stability as function of time, acc. to MIL-Std 202, Method 108, Condition D (after 1000h)

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Thin Film Contact Systems

on resistive and adhesive layer or substrate

Product Specification — *Data Sheet No. RMT-SH-A-681-01-010407*

CONTACT SYSTEMS on resistive layer or substrate [1]

Standard Systems	Base						Properties		
Heat treatment	Sub. + Ta	Sub. + NiCr	Bare Sub.	Minimum required (Adhesion)	Max.Long Term (Stabilis.)	Max. Short Term (Assembly)	Soldering[3] MIL-Std 883 Method 2003	Wire Bonding[4] MIL-Std 883 Method 2011	Adhesion MIL-Std 883 Method 2027
TiW + Au		✓	✓ [5]			450°C/5Min	not recommended	✓	✓
TiW + Pd + Au	✓	✓	✓ [5]					✓	✓
Ti + Pd + Au		✓	✓ [5]		350°C/2h		✓	✓	✓
Pd + Au		✓		250°C/1h		400°C/5Min		✓	✓
NiV + Au		✓						min.2,0µm Au	✓
Ti+Cu+Ni+Au		✓	✓ [5]		250°C/2h	350°C/5Min	✓	✓	✓
CrXB+TiW+Pd+Au			✓ [6]		350°C/1h	400°C/5Min	✓	✓	✓
CrXB+Ti+Pd+Au			✓ [6]		300°C/1h	350°C/5Min	✓	✓	✓
CrXB+Pd+Au			✓ [6]		250°C/1h	300°C/5Min	min.2,0µm Au	min.2,0µm Au	✓

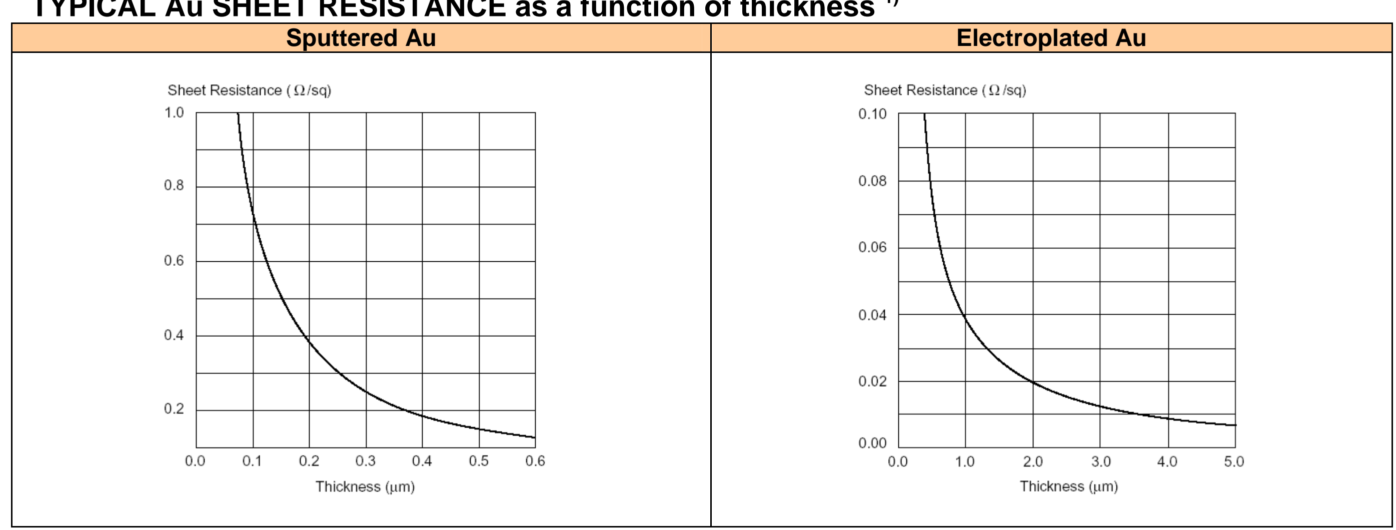
SPUTTERED LAYERS [1]

Standard values	Adhesion layers			Barrier layers				Conductive layers	
	CrXB	NiCr	Ta_2N	Ti	TiW	NiV	Pd	Au	Cu
Nominal Thickness [nm]	90	50	50	60	25-60	150	100	100	600
Tolerance to nominal	± 10 %								
Spread within substrate	± 5 %								

ELECTROPLATED LAYERS [1] [2]

Standard values	Full metallized	Patterned				
	Au	Au	Cu	Ni		
Nominal Thickness [µm]	2 - 10	2 - 100	3 - 150	1 - 5		
Tolerance to nominal	±20%	±30%	±50%	±70%		
Spread within substrate	±10%	n/a	n/a	n/a		

TYPICAL Au SHEET RESISTANCE as a function of thickness [1]



1) Guaranteed up to 5mm from the edge of the metallised substrate.
2) Electroplated thickness guaranteed on reference side only. Thickness on the opposite side can be guaranteed first after qualification run.
3) For substrate surface roughness 1µ" or less min. 0.3 µm Au required / For substrate surface roughness above 1µ" min. 1.0 µm Au required
4) Minimum 1.0 µm Au required
5) Alumina and Aluminum nitride, as fired, lapped or polished
6) Quartz, Sapphire, Glass, Silicon Wafer oxidized

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Design Rules
for thin film substrates

REQUIRED DATA

1. Circuit drawing	Containing the data below
2. Resistor	a. Nominal values and other relevant parameters b. Absolute tolerances c. Ratio tolerances and reference resistor
3. Chip dimensions	a. Nominal values b. Tolerances
4. Resistive layer type	See section "Resistive and conductive layers" and corresponding detailed data sheets in our "Product Specification"
5. Conductor layer(s)	
6. Substrate type	
7. Electronic data (listed formats, preference a→d)	a. DWG b. DXF c. GDS II d. Graffy, Gerber extended

SUBSTRATE MACHINING (ceramics only)

Typical values	**Hole exit diameter D** [µm]			**Cut locations and distances** [µm]			**Scribe & snap** [mm]	
Substrate thickness	Standard	Minimum	Taper T	Gen.Tol. a,b,c,d,e	Cut to pattern e,f	Cut to cut g,h,i	Min. Dim.	Min. Tol.
0.005"	200	150	Max. 10% of substrate thickness	± 50	50	Min. = substrate thickness	3 x 3	± 0.05
0.010"	250	150					3 x 3	
0.015"	300	200					4 x 4	+0.15 / -0.05
0.025"	400	300					4 x 4	
	T, E, D ± 0.05 mm			scribe&snap, slot, pattern, profile, slotted vias, a, b, c, d, e, f, g, h, i			Scribe depth 30-50% a, b, c Scribe line to scribe line prior to breaking a, b, c ± 0.05 mm Spacing 0.15±0.025 mm	

RESISTIVE LAYERS AND CONTACT SYSTEMS

Typical values	**Resistive layers (Ω/□)**		**Contact System (spt) [nm] ± 10%**						**Contact system (elp) [µm]**		
	NiCr	Ta_2N [1)]	Ti	TiW	NiV	Pd	Au	Cu	Au ±30%	Cu ±50%	Ni ±70%
Ceramics as fired	20 - 250	20 - 150	60	25-60	150	100	100	600	2 - 100	3 - 150	1 - 5
Glass & polished ceramics	20 - 300	20 - 150									
Si Wafer	20 - 300	-									

1) on glass not recommended

LINEWIDTH AND SPACING

Typical values (µm)	**Resistor and conductor**		**Metallization around vias** [2)]		**Conductor size tolerances**		
	Standard	Minimum	Standard	Minimum	Standard	Minimum	Partial
Ceramics as fired	50	20	100	50	± 10	± 5	± 3
Glass & polished ceramics							
Si Wafer	20	10					

2) via size differences on front and back side to be taken into account

CHIP SIZE AND PATTERN ALIGNMENT [3)]

Typical values (µm)	Chip size tolerances		Pattern pullback A-side		Pattern pullback B-side		Alignment A to B pattern	
	Standard	Minimum	Standard	Minimum	Standard	Minimum	Standard	Minimum
Ceramics as fired	±50	±25	100±50	25±25	100±100	50±50	±50	±25
Glass & polished ceramics								
Si Wafer								

3) chip size to be designed on a 5µm grid

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Design Rules
for thin film substrates

DESIGN OF TRIMMED RESISTORS

all data in µm	Top hat width	Ladder window size Length x Width		Minimum block resistor size			
				Length < Width		Length > Width	
		Standard	Minimum	Length	Width	Length	Width
Ceramics as fired Glass & polished ceramics Si Wafer	2 x LW + 20	50	20	50	100	100	50
Value before trimming	30% below the nominal			20% below the nominal			
Trimming range	up to 30% above the nominal			n/a			

DC Trimming			I-cut	Ladder-cut	I-cut	L-cut
Range	Accuracy Std.	Accuracy Min.	LW	LxW	C R	C R
5Ω-1 MΩ	± 1%	±0.05%				
RF Trimming					Edge-trim	Edge-trim
Range	Accuracy Std.	Accuracy Min.	N/A	N/A	Symetric edge cut Symetric window cut Asymetric edge cut	
5Ω-1 MΩ	± 5%	±1%				
No Trimming						
5Ω-1 MΩ	±20%		N/A	N/A	Length x Width to be minimum 100µm	

Rules for resistor trimming

1. Ladder windows to be designed in 2,5µm grid with equivalent size within one ladder.
   For different types of ladder (coarse, fine) the cut length may vary.
2. All areas to be trimmed shall be perpendicular to each other (as standard).
3. Resistor test points to be minimum 100 x 100 µm additionaly to the bonding area.
   Minimum pad size required 250x250 µm.
4. The maximum possible change in any trimming step (coarse ladder, fine ladderr, top hat) must be at least by 20% greater than the smallest possible change in the previous trimming step (e.g. a 5% change per one ladder cut means that the next trimming in top hat must allow at least 6% change).
5. The last trim cut must take into account the final required tolerance, i.e. a 2,5 µm cut step must not cause value change greater than 20% of the required final tolerance
6. For low resistor values in particular the resistance and the TCR of the connections must be considered
7. For resistor sizes below 100µm design correction shall be taken into account.
8. For resistors in loop (minimum three resistors) the achievable tolerances are dependent on the resistors ratio.
9. Two parallel resistors can be neither measured nor trimmed. In such cases it is recommended to add separated test resistors having the same design as the resistors to be guaranteed.

PASSIVATION / SOLDER-STOP

Material	Edge accuracy µm	Thickness µm	Passivation	Solder stop	Material	Edge accuracy µm	Thickness µm	Passivation	Solder stop
Photoresist	10	1 - 5	✓	240°C	Glass paste	100	20	✓	475°C
Polyimide	25	1 -10	✓	360°C	Ni-Oxid	5	n/a	-	360°C
Dry Film	10	~37	-	240°C					

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Design Rules
for special applications

POLYIMIDE SUPPORTED BRIDGES

Materials and Properties		Dimensions and Tolerances	
Conductor	Au	Length (min,)	60 µ
Support	Polyimide	Width (min.)	35 µ
Coupler line (min.)	20 µm	Height	~ polyimide thickness
Coupler space (min.)	20 µm	Thickness	5 – 10 µm
		Polyimide thickness	3 – 5 µm

AIR BRIDGES

Materials and Properties		Dimensions and Tolerances	
Conductor	Au	Aspect Ratio L:W (max.)	6:1 (unsupported area)
Coupler line (min.)	25 µm	Width (minimum)	25 µm
Coupler space (min.)	25 µm	Length (minimum)	75 µm
Height (maximum)	5 – 10 µm	Thickness	8 µm ± 30%

FILLED VIAS - for better thermal and electrical conductivity front to backside

Materials and Properties		Dimensions and Tolerances	
Substrate	Alumina Al_2O_3 - 99,6%, ALN	Surface Finish	Lapped, Ra < 0,6 µm
Thickness	0.010" and 0.015"	Via diameter	300 – 400 µm
Conductive Layer	Barrier Layer + Au elp 5 ± 1,5 µm	Oval Via diameter	700 x 400 µm
Resistive Layer	NiCr or Ta_2N, 50 Ohm/sq. typical	Capture pad	hole diameter + 100 µm
Fill Material	Solid Cu	Via to via pitch	Via diameter + 100µm
Via electrical resistance	n/a	Via location tolerance	± 25 µm
Via Thermal Conductivity	380W/m·K typical	Via diameter tolerance	± 25µm

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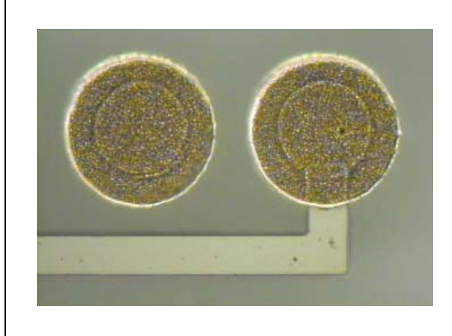
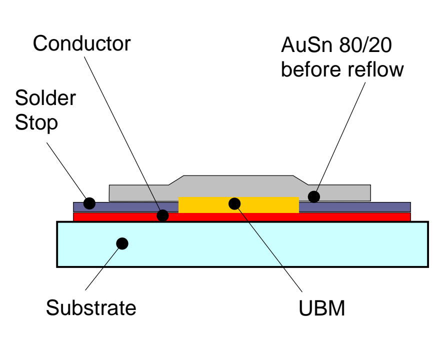
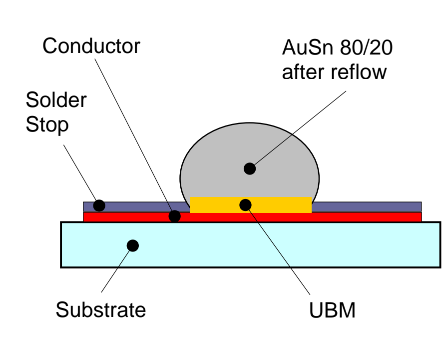
EVAPORATED SOLDER BUMPS (AuSn or Sn) – for flux free soldering in optoelectronics

Materials and Properties		Dimensions and Tolerances	
Eutectic solder	Au (80%)+Sn (20%)	AuSn deposited thickness	5.2 µm ± 25%
Soldering temperature	300 – 320 °C	Bump height (reflowed)	10 – 40 µm ± 30%
Solder	Sn	Pad size (diameter)	40 – 100 µm ± 5µm
Soldering temperature	240 °C	Pitch (min.)	80 µm

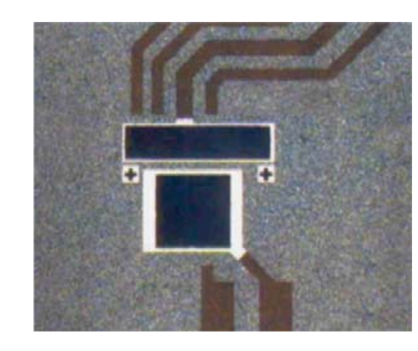




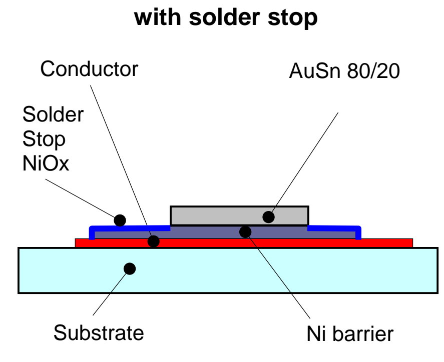


EVAPORATED SOLDER PADS (AuSn or Sn) – for flux free soldering in optoelectronics

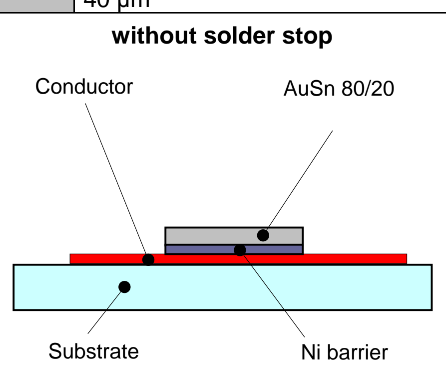
Materials and Properties		Dimensions and Tolerances	
Eutectic solder	Au (80%)+Sn (20%)	AuSn deposited thickness	5.2 µm ± 25%
Soldering temperature	300 – 320 °C	Pad size tolerance	± 5 µm
Solder	Sn	Pad size (min.)	20 µm
Soldering temperature	240 °C	Pitch (min.)	40 µm



with solder stop



without solder stop



LASER REFLOWED SOLDER BUMPS (SnPb) – for flip chip soldering in microelectronics

Materials and Properties		Dimensions and Tolerances	
Eutetic solder	Sn (63%)+Pb (37%)	Pad size (diameter)	min. 50 / up to 500 µm
Soldering temperature	220 - 240 °C	Bump height (reflowed)	min. 95 / up to 680 µm
Underbump metallisation	UBM suitable for soldering	Pitch (min.)	200 µm / up to 1000 µm

Solder Bumping

Conductor
After reflow
Solder mask
SnPb (63/37)
Substrate
UBM

Features not covered herein might be available on request.

This specification is subject to change without notice

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thin film technology for microelectronics

Thin Film Products
Production and Quality Control
Metallized Substrates

General Information — *Data Sheet No. RMT-SH-A-324-02-010407*

All products are manufactured according to customer specification using qualified materials and processes. Each production lot is tested by qualified personnel during the production as well as quality-controlled and certified by Quality Assurance prior to delivery.

Production Controls	**Sputtered Layers**	**Inspection plan**
	☑ **Incoming inspection** of substrates	Level I AQL 2,5
	☑ **Visual inspection** after metallization	100%
	☑ **Electrical tests** (destructive): Sheet resistance (if applicable) TCR two-point test <20/100°C> (if applicable)	Level S1 AQL 6,5 (every metallization lot)
	☑ **Adhesion test** (glass, quartz and polished alumina only)	1 Substrate/lot
additional for	**Electroplated layers** acc. to ASTM B488-01, Type III/A (MIL-G-45204C canceled)	
	☑ **Visual inspection** after electroplating	100%
	☑ **Layer thickness** measurement (nondestructive)	100%

Quality Control	**Sputtered Layers**	**Inspection plan**
	☑ **TCR(T)** as a function of temperature within -55 to 150°C according to MIL-STD-202: Method 304	1 substrate per five lots (minimum 1 s. per order)
	☑ **LTS(t)** as a function of time (1000 h) at elevated temperature according to MIL-STD-202: Method 108, Condition D	1 substrate per five lots (minimum 1 s. per order)
additional for	**Electroplated layers**	
	☑ **Visual inspection**	Level II AQL 1,0
	☑ **Layer thickness** measurements	Level S1 AQL 1,0
	☑ **Visual inspection** after heat treatment 2 h @ 350°C (destructive)	Level S1 AQL 1,0
on request	☒ **Bond Strength Test** (Electroplated layers only) according to MIL-STD-883: Method 2011 Condition D	Level S1 AQL 1,0
	☒ **Adhesion Pull Test** according to MIL-STD-883: Method 2027	Level S1 AQL 1,0

QA Records with delivery	Certificate of Compliance	
	Electrical Data Record	(if applicable)
	TCR Record (Temperature Coefficient of Resistance)	(if applicable)
	Electroplated Layer Thickness Record	(if applicable)
on request	☒ Bond Strength Test Record	
	☒ Pull Test Record	
	☒ LTS Record (Long Term Stability), available two months after the delivery	

Quality System Provisions	Sampling plan according to MIL-STD-105 (DIN 40080)
	Traceability for each production lot and sputtering/electroplating batch.
	Production is supported and audited by QA department.

Quality System is certified to ISO 9001:2000 (Reg. No. 10512)

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Thin Film Products
Production and Quality Control
Patterned Substrates

General Information — *Data Sheet No. RMT-SH-A-325-02-010407*

All products are manufactured according to customer specification using metallized substrates tested according to RMT-SH-A-324. Each production lot is tested by qualified personal during the production as well as quality-controlled and certified by Quality Assurance prior to delivery.

Production Control	☑	**Visual inspection** after each production step	Level II	AQL 6,5
	☑	**Electrical tests** - Lithography	Level S1	AQL 6,5
	☑	**Electrical tests** - Trimming	Level S1	AQL 1,5
	☑	**Dimensional tests** - Lithography	Level S1	AQL 6,5
	☑	**Dimensional tests** - Dicing	Level S1	AQL 6,5
	☑	**Final visual inspection** according to MIL-Std 883, Method 2010 and 2032	100 %	

Quality Control	☑	**Visual inspection** (MIL-Std 883C)	Level II	AQL 1,0
	☑	**Electrical tests**	Level S1	AQL 1,0
	☑	**Dimensional tests**	Level S1	QL 1,0
	☑	**TCR(T) *)** as a function of temperature within -55 to 150°C according to MIL-STD-202: Method 304	as per RMT-SH-A-324	
	☑	**LTS(t) *)** as a function of time at elevated temperature according to MIL-STD-202: Method 108, Condition D	as per RMT-SH-A-324	
	☑	**Sample stock**	2 to 5 chips per lot	
on request	☒	**Bond Strength Test** (electroplated gold only) according to MIL-STD-883C: Method 2011, Condition D	Level S1	AQL 1,0
	☒	**Adhesion Pull Test** according to MIL-STD-883: Method 2027	Level S1	AQL 1,0

***)** Tests are done by using a test pattern on the substrate from the same lot.

QA Records
- Certificate of Compliance

on request
- TCR Record (Temperature Coefficient of Resistance)
- Bond Strength Test
- Pull Test Record
- Inspection Survey confirming all performed control steps
- LTS Record (Long Term Stability), available two months after the delivery

Quality System Provisions
- All sampling plans according to MIL-STD-105 (DIN 40080)
- Traceability for each production lot and sputtering batch.
- Production is supported and audited by QA department.

Quality System is certified to ISO 9001:2000 (Reg. No. 10512)

Features not covered herein might be available on request.
This specification is subject to change without notice

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Certificate

SQS herewith certifies that the company named below has a management system which meets the requirements of the normative base specified below.

Reinhardt Microtech AG
CH-7323 Wangs

Certified area

Whole Company

Field of activity

Thin Film Technology

Normative base

ISO 9001:2008 Quality Management System

Swiss Association for Quality and
Management Systems SQS
Bernstrasse 103, CH-3052 Zollikofen
Issue date: October 31, 2009

This SQS Certificate is valid up to
and including October 30, 2012
Scope number 19
Registration number 10512

X. Edelmann, President SQS

T. Zahner, Managing Director SQS

SCESm 001

Swiss Made