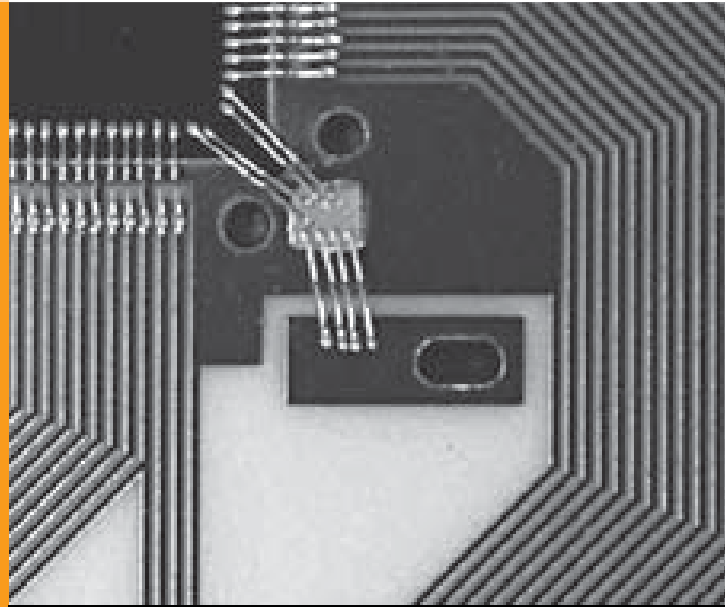




# Design Manual



Thick Film

Thin Film

RF-PCB

Assembly/Packaging

Screening/Test

The following rules are effective for the draft of circuit boards and hybrid assemblies. The instructions are only valid for the layout design at RHe Microsystems GmbH. The rules are not intended to be exhaustive. All layouts should be designed in a close collaboration with RHe Microsystems GmbH.

Data file formats: GDS II, DXF, DWG, Extended GERBER (274-X) others on request

Compliance with mentioned values is depending on the properties of the used base material. A consultation is recommended.

## **Standard**

These standard values can be used as a base for your layout and design process without request at RHe.

## **Special**

These values are achievable by using special materials and/or special manufacturing equipment and methods. In any case a request for feasibility at RHe is recommended during early development/layout stage.

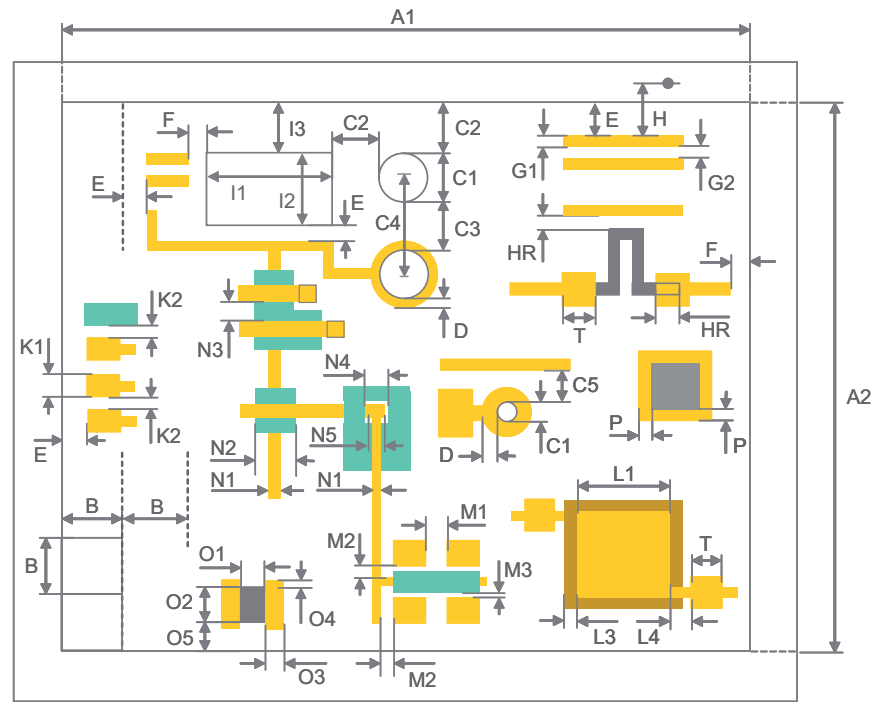
Special values should only be requested if a solution can't be found by using standard values.

## **Development**

In this column named values are mostly custom made designs. As a developer/project leader please consider feasibility studies or separate sample manufacturing and use these parameters only in a tight collaboration with RHe in your products and constructions.

We look forward to be your partner for your special project. The manufacturing technologies will be especially designed to your requirements and series quantities.

# Thin Film Drawing



Please note:

The drawing is a summary of all elements from thick film and thin film.

Because of this the selected design rule table below does not include all elements of the drawing.

Details for Resistors and Polyimid (Capacitors, Multilayer, Bridges etc.) please see separate table in chapter Thin Film metallisation.

# Thin Film Design rules

		Standard	Special	Development
A1/A2	Tile dimension: 4" x 4", usable area:	88.0 x 90.0 mm <sup>2</sup>	92.0 x 92.0 mm <sup>2</sup>	x
A1/A2	Tile dimension: 2" x 2", usable area:	46.8 x 46.8 mm <sup>2</sup>	x	x
B	Dimension of single circuit boards on a tile:			
	Separation by laser scribing and breaking	≥ 3.0 x 3.0 mm <sup>2</sup>	≥ 2.0 x 1.5 mm <sup>2</sup>	
	Separation by sawing / dicing	≥ 2.0 x 2.0 mm <sup>2</sup>	≥ 1.5 x 0.6 mm <sup>2</sup>	
	Width of dicing channel (no metallisation in the channel allowed)	0.140 mm		
	Tolerances of single circuit board dimensions			
	Separation by sawing (after patterning)	± 0.050 mm	± 0.025 mm	± 0.015 mm
	Separation by scribing and breaking (after patterning)			
	Substrate thickness: ≤ 0.381 mm	+ 0.100 / - 0.025 mm		
	Substrate thickness: ≤ 0.635 mm	+ 0.150 / - 0.050 mm		
	Substrate thickness: ≤ 1.270 mm	+ 0.200 / - 0.050 mm		
	Tolerance scribing line to scribing line	≤ ± 0.035 mm	≤ ± 0.020 mm	
C1	Drilled hole / PTH: Ø (measured at laser exit, laser entrance + 7 ... 10%)	≥ 0.200 mm	≥ 0.150 mm	x

		Standard	Special	Development
C1	Min. ratio drilled hole to substrate thickness:	$\geq 0.5$	$\geq 0.5$	
	Tolerance drilled hole dimension	$\pm 0.035$ mm	$\pm 0.025$ mm	
C2	Distance hole circumference to substrate edge or cut-out	$\geq$ Substrate thickness		
C3	Distance hole circumference to another hole circumference	$\geq$ Substrate thickness	$\geq 0.8 \times$ Substrate thickness	
	Tolerance hole true center to another hole true center	$\leq \pm 0.020$ mm		
	Tolerance hole true center to another hole true center, substrate stress annealed	$\leq \pm 0.035$ mm		
D	Metallisation ring (rim) around a drilled hole on top and bottom	$\geq 0.100$ mm	$\geq 0.070$ mm	x (0 – 0.05 mm)
E	Distance conductor to substrate edge:			
	Separation by scribing and breaking	$\geq 0.200$ mm	$\geq 0.100$ mm	
	Separation by sawing / dicing	$\geq 0.100$ mm	$\geq 0.050$ mm	$\geq 0.010$ mm
	Distance conductor parallel to substrate edge or cut-out edge	$\geq 0.200$ mm		$\geq 0.150$ mm
F	Distance conductor orthogonal to substrate edge or cut-out edge	$\geq 0.150$ mm	$\geq 0.100$ mm	$\geq 0.050$ mm
G1/G2	Conductor Line & Space: *			
	Cu conductor width, Cu thickness 3 - 6 $\mu$ m	0.050 mm	0.030 mm	0.020 mm
	Tolerance conductor width: Cu thickness up to 3 $\mu$ m / 10 $\mu$ m	$\pm 0.005$ mm / 0.007 mm	$\pm 0.003$ mm / 0.005 mm	
	Au conductor width, Au thickness up to 3 $\mu$ m*	0.040 mm	0.025 mm	0.010 mm
	Tolerance conductor width: Au thickness up to 3 $\mu$ m / 10 $\mu$ m	$\pm 0.003$ mm / 0.005 mm	$\pm 0.002$ mm / 0.005 mm	$\pm 0.002$ mm / 0.004 mm
	Resistors and adhesive layer, with tolerance of $\pm 3$ $\mu$ m	0.040 mm	0.015 mm	
H	Alignment tolerance conductor to laser fiducial	$\pm 0.030$ mm	$\pm 0.020$ mm	
	Alignment tolerance top to bottom patterning	$\pm 0.060$ mm	$\pm 0.030$ mm	
HR	Alignment tolerance resistors to conductor	$\pm 0.020$ mm	$\pm 0.050$ mm	x
I1/I2	Cut-outs (parallel to substrate edge)			
	Dimensions (measured at laser exit, laser entrance + 7 ... 10%)	$\geq 1.000$ mm x 1.000 mm	$\geq 0.500$ mm x 0.500 mm	x
I3	Distance cut-out to substrate edge or another cut-out edge	$\geq$ Substrate thickness		
	Alignment tolerance cut-out to substrate edge cut or sawn	$\pm 0.050$ mm	$\pm 0.020$ mm	
	Alignment tolerance cut-out substrate edge scribed/broken**	+ 0.250 / - 0.100 mm		
I1/I2	Cavity (parallel to substrate edge)			
	Dimension (related to cavity base)	$\geq 1.000$ mm x 1.000 mm	$\geq 0.500$ mm x 0.500 mm	x
	Remaining substrate thickness in cavity / cavity base	$\geq 0.130$ mm	x ( $\geq 0.100$ mm)	
I3	Distance cavity edge to substrate edge	$\geq$ Substrate thickness		
	Tolerance cavity to substrate edge sawed	$\pm 0.050$ mm	$\pm 0.020$ mm	
K1	Wire bonding pad dimension: Standard	$\geq 0.300$ mm x 0.300 mm	x	
K1	Wire bonding pad: Parallel to wedge wire bonding direction	$\geq 0.250$ mm x 0.050 mm	x	
	Distance wire bonding pad to other pad types/solder stop	$\geq 0.250$ mm		
T	Pad dimension for electrical measurements and laser trimming of resistors	$\geq 0.300$ mm x 0.300 mm	$\geq 0.250$ mm x 0.250 mm	x
M1	Distance between two adjoining solder pads	$\geq 0.500$ mm	$\geq 0.250$ mm	
M2	Distance solder pads to conductor without covering	$\geq 0.500$ mm	$\geq 0.300$ mm	
	x on request			
	* depending on metallisation material, thickness, location and frequency of occurrence of conductive tracks as well as surface quality of substrate			
	** depending on substrate thickness			

# Thin Film metallisation

Metallisation Systems *							Processing				
Resistor	Adhesive layer	Barrier layer	Conductive layer	Barrier layer	Surface	Solder stop	Standard solder material 1)	Special solder material	Au wire bonding	Al wire bonding	Gluing
(TaN)***	TiW (50 nm)		Au (1.5 ... 10 µm)**			Polymer, TiW		x	x		x
(TaN)***	TiW (50 nm)	Pd (250 nm)	Au (1.5 µm)			Polymer, TiW	x*		x		x
(TaN)***	TiW (50 nm)		Au (1.5 ... 10 µm)**	Ni (1.5 ... 5 µm)	Au (0.1 ... 0.2 µm)	Polymer, TiW	x	x		x	x
(TaN)***	TiW (50 nm)		Au (1.5 ... 10 µm)**	Ni (1.5 ... 5 µm)	Au (0.9 ... 1.2 µm)	Polymer, TiW	x	x	x		x
(TaN)***	TiW (50 nm)		Au (1.5 ... 10 µm)**	NiP (2 ... 5 µm)	Au (0.05 ... 0.1 µm)	Polymer, TiW	x	x		x	x
	(TiW (50 nm) )		Pt (25 nm ... 800 nm)								x
(CrNi)***	TiW (50 nm)		Au (1.5 ... 10 µm)**			Polymer, TiW		x	x		x
(CrNi)***	TiW (50 nm)	Pd (400 ... 600 nm)	Au solder pads (0.05 ... 0.1 µm) and Au wire bonding pads (5 µm) selective			Polymer, TiW	x*		x		x
(CrNi)***	CrNi (50 nm)		Cu (3 ... 10 µm)	Ni (1.5 ... 5 µm)	Au (0.1 ... 0.2 µm)	Polymer	x			x	x
(CrNi)***	CrNi (50 nm)		Cu (3 ... 10 µm)	Ni (1.5 ... 5 µm)	Au (0.7 ... 1.2 µm)	Polymer, NiO	x	x	x		x
(CrNi)***	CrNi (50 nm)		Cu (3 ... 10 µm)	Ni (1.5 ... 5 µm)	Au (1.2 ... 1.8 µm)	Polymer, NiO		x	x		x
	CrNi (50 nm)		Cu (3 ... 10 µm)	NiP (2 ... 5 µm)	Au (0.05 ... 0.1 µm)	Polymer	x	x		x	x

Metallisation Systems as multilayer *											
Resistor	Adhesive layer	1. Conductive layer	Isolation	2. Conductive layer	Barrier layer	Surface					
(TaN)***	TiW (50 nm)	Au (1.5 ... 5 µm)**	Polyimid (3 ... 5 µm)	TiW/Au (1.5 ... 10 µm)**	Ni versions	Au version	x	x	x		x
	* Tolerance layer thickness: ± 20 %										
	** selective reinforcement of Au possible										
	*** if resistors required (in case of CrNi resistors adhesive layer n.a.), layer thickness depending on R <sub>sq</sub>										
	x* containing Pb										
	1) Pb free, Ni ≥ 3 µm										

Resistors				
TaN	High stable	TCR: - 90 ppm / K ± 40 ppm / K		Tracking: < 5 ppm / K
CrNi	TCR adjustable	TCR adjustable between - 20 ppm / K and + 60 ppm / K		Tracking: < 5 ppm / K
Square resistance R <sub>sq</sub>		20 Ω, 50 Ω, 100 Ω, tolerance: ± 15 %; 200 Ω, tolerance: ± 30 %		
Rectangular resistors:		R = RL * R <sub>sq</sub> / RW		
Resistor geometry: Length > width		RL: ≥ 0.100 mm	RW: ≥ 0.050 mm	
Resistor geometry: Length < width		RL: ≥ 0.080 mm	RW: ≥ 0.150 mm	
Meander resistors:			RW: ≥ 0.050 mm	As „special“: min. RW: ≥ 0.030 mm
Distance between adjoining resistors			≥ 0.050 mm	
Overlapping zone resistors with conductive tracks RÜ		Standard: ≥ 0.100 mm	Special: ≥ 0.050 mm	RG: Opposite resistors with shared overlapping zone
Conductive track width at resistor overlapping zone RÜB		Ta-N-R: Double-side over RB each ≥ 0.020 mm; CrNi-R at Cu layer: 0 μm; CrNi-R at Au layer: 50 μm		
Laser trimming: Geometry / dimensions			RW: ≥ 0.100 mm	Resistance 75 – 80 % of final value
Distance between resistors laser trimmed			≥ 0.150 mm	
Pad dimension for measurements and laser trimming		≥ 0.300 mm		As „Special“: min. ≥ 0.250 mm
Tolerance after laser trimming		Standard: 1%	Special: ≥ 0.5 %	Development: ≥ 0.1 %, depending on resistor geometry
Long-term stability at R <sub>sq</sub> 20 Ω, 50 Ω, 100 Ω		≤ 0.5 %		
Heat dissipation / power loss		≤ 150 mW / mm <sup>2</sup> (at ~ 130°C, on Al <sub>2</sub> O <sub>3</sub> )		Depending on ceramic material, geometry and surrounding
Temperature load		max. 150 °C, constant		

Polyimide on Au conductive layer			Calculation of capacitors	
Layer thickness	3 ... 5 μm		$C_{\text{Polyimid}} = \epsilon_0 \cdot \epsilon_r \cdot A / d$	d = layer thickness polyimide A = overlapping area L (Area capacity coating)
Line width	≥ 0.050 mm		$\epsilon_0 = 8.85 \cdot 10^{-12} \text{ [F / m]}$	
Distance between polyimide patterning	≥ 0.050 mm		$\epsilon_r = 3.2 \dots 3.3 \text{ (0 \% ... 50 \% RH)}$	
Vias in polyimide	≥ 0.100 mm x 0.100 mm / standard		≥ 0.050 mm x 0.050 mm / special	for multilayer
L1	Dimensions of capacitor plates on substrate and polyimide	minimal ≥ 0.050 mm x 0.050 mm		Used for: Solder stop, glue stop, conductive track cross over, multilayer, bridges, capacitors
L3	Overlapping of polyimide on capacitor plate	≥ 0.100 mm / standard	≥ 0.050 mm / special	
L4	Distance pads for capacity measurement to capacitor plate	≥ 0.100 mm / standard	≥ 0.050 mm / special	
T	Pad dimension for capacity measurement	≥ 0.400 mm x 0.400 mm	≥ 0.300 mm x 0.300 mm	
	Patterning mismatch upper capacity coating	± 0.020 mm		

# Thin Film materials

Ceramic material	Composition	Dielectric Constant $\epsilon_r$ @ 25 °C]	Loss Tangent [tan $\delta$ @ 1MHz]	Thermal Conductivity [W / mK @ 25 °C]	Coefficient of linear Thermal Expansion CTE [ppm / K]	Dielectric Strength [kV / mm]	Density [ $\rho$ / cm $^3$ ]	Surface finish typical Ra [nm]	Thickness **										Processing						
									0.127 mm	0.178 mm	0.254 mm	0.381 mm	0.504 mm	0.635 mm	1.016 mm	1.270 mm	Laser drilling	Laser cutting	Cavity	Laser scribing	Sawing/Dicing				
Aluminium oxide ceramic 99,6 % (Al $_2$ O $_3$ )	as fired	9.9	0.0001	35	7	12	3.88	50 ... 100	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x
Aluminium oxide ceramic 99,6 % (Al $_2$ O $_3$ )	polished	9.9	0.0001	35	7	12	3.88	5 .. 20	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x
Aluminium oxide ceramic 99,6 % (Al $_2$ O $_3$ )	TPS polished	10.1	0.0001	35	6.3	12	3.95	$\leq$ 26	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x
Aluminium nitride ceramic (AlN)	as fired	8.9	0.001	170 - 190	4.6	20	3.30	$\leq$ 600				x	x	x	x	x	x	x	x	x	x	x	x	x	x
Aluminium nitride ceramic (AlN)	lapped	8.9	0.001	170 - 190	4.6	20	3.30	$\leq$ 600				x	x	x	x	x	x	x	x	x	x	x	x	x	x
Aluminium nitride ceramic (AlN)	polished	8.9	0.001	170 - 190	4.6	20	3.30	100				x	x	x	x	x	x	x	x	x	x	x	x	x	x
Calcium magnesium titanate (CaMgTiO $_3$ )	polished	19.5	0.0002	4.2	8.6		3.80	13				x	x					x							x
Saphir	polished	10.0	0.0001	42	5	48	3.97											(x)	(x)						x
Quartz glass SiO $_2$ *	lapped	3.8	0.001	1.46	0.6	30	2.20	50 ... 1000			x	x						(x)	(x)						x
Quartz glass SiO $_2$ *	polished	3.8	0.000015	1.46	0.6	30	2.20	5 ... 20			x	x						(x)	(x)						x
Zircon substrate	as fired	11.0	0.0005	27	8		4.07	30 ... 130				x	x												x
Low alcali borosilicate glass / glass AF 45		6.2	0.0009	1	4.5	38	2.72				0.2	0.3	0.4	0.5	0.7				x						x
Dielectric materials and other ceramics ***		36 ... 100																							x
Microwave ferrite																		x							x

\* Manufacturing only by order

\*\* Thickness-Tolerance: Standard  $\pm$  10 %, premium  $\pm$  5 %; other thickness in compliance with customer request

\*\*\* Dielectric materials and other ceramics in compliance with customer request

(x) extern in Cicor Technologies Group



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